REMARKS

Claims 1 through 5 remain pending in the application. In response to the Office Action,

dated October 19, 2004, a new title has been provided. In addition, claim 1 has been amended.

Care has been taken to avoid the introduction of new matter. Favorable reconsideration of the

application is respectfully solicited.

Claims 1 through 5 have been rejected under 35 U. S. C. § 102(b) as being anticipated by

U.S. Patent 5,877,976 (Lattimore). The Office Action refers to Fig. 6 of Lattimore for schematic

representation of a multiport memory cell. Fig. 10C has been referred to for the arrangement of

word lines. It is submitted that Lattimore does not disclose the requirements of claims 1 through 5.

Independent claim 1 recites, in part, the following:

> each of said plurality of first word lines and each of said
> plurality of second word lines are arranged alternately in a planar
> layout.

This recited arrangement corresponds to description of Fig. 3 in the specification at page 7.

As described, "each of word lines WLA0-WLA2, electrically connected to the first port and each of

word lines WLB0-WLB2, electrically connected to the second port, are arranged alternately in the

planar layout. In other words, the word lines are planarly arranged in the order of word line WLA0,

word line WLB0, word line WLA1, word line WLB1, word line WLA2, and word line WLB2, from

above in Fig. 3." This arrangement is then contrasted with circuit configuration of Fig. 4, in which

word lines connected to the same port are adjacent to each other.

Independent claim 4 recites, in part, the following:

> in a first row and a second row adjacent to each other, said
> word line in said first row and said word line in said second row are
> adjacent to each other, and in said second row and a third row
> adjacent to each other, said match line in said second row and said
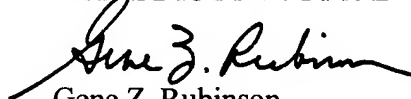> match line in said third row are adjacent to each other.

Fig. 6 of Lattimore depicts a single cell of a single row. Port 1 word line is configured along the upper portion of the cell and port 2 along the bottom. Fig. 10 is a topological representation of a portion of two adjacent rows of the cell array. The port 2 word lines of the rows are adjacent each other. There is no port 1 word line interspersed between the two adjacent port 2 word lines. There is nothing in Lattimore that teaches that each of the plurality of first port word lines and are arranged alternately with each of the plurality of second port word lines as would be required by independent claims 1 and 4.

Accordingly, it is submitted that there is no anticipation of claims 1 through 5 by Lattimore. Allowance of the application is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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